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DESIGN OF RING OSCILLATOR USING CS-CMOS FOR MIXED SIGNAL SOCs

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ABSTRACT

This paper reports design of a ring oscillator using CS-COMS low noise logic family for mixed signal SOCs. Design has been implemented using 180nm technology with 1.8V supply voltage using CS- CMOS logic. CS-CMOS logic efficiently reduce switching noise while maintaining the speed as compare to the other logics like CSL, CBL etc.

After completion of the design authors have simulated the design in Spectre simulator and obtained the best simulation results. Authors have determined the parameters like phase noise, delay.

KEYWORDS: Cadence, Current Balanced Logic (CBL), Current Steering CMOS (CS-CMOS), Current Steering Logic (CSL), Mixed Signal SOCs, Ring Oscillator, Spectre Simulator

INTRODUCTION

Design a ring oscillator circuit in VLSI using CMOS will give high packing density and low power consumption and are easy to design [1],[2]. Most of the power consumed by CMOS gates is due to displacement currents [3] drawn during state-transitions for charging and discharging wire and device capacitances.

These increase linearly with the operating frequency and flow through the power supply wires, ground lines, parasitic inductances and capacitances causing ringing and voltage drop. This is the dominant source of substrate noise [4].which causes phase noise in ring oscillator resultant jitter PLL.

The problem of switching noise in ring oscillator can be deal by designing a ring oscillator using current steering logic, such as current steering logic (CSL), current-balanced logic (CBL), here present a new logic family called the current-steering CMOS (CS-CMOS) [1] obtained by a simple modification keeping the core CMOS structure intact to preserve its most attractive features.

This family not only reduces the switching noise but also delivers higher speed than CSL and CBL for the same power consumption. Designing of ring oscillator using CS-CMOS will give better phase noise compare to CSL and CBL logic.

CS-CMOS LOGIC

CS-CMOS is obtained by a simple current-steering modification to the standard CMOS family. As in a CMOS inverter, a pair of complimentary transistors connected in series forms the core of the proposed CS-CMOS inverter, as shown in Figure.1.

Since CMOS gates do not draw any appreciable current in their static states, constant-current operation requires additional paths for the dc bias current to flow. A pair of complimentary transistors is added in parallel for this purpose. A P-channel transistor sources a constant current to each gate.

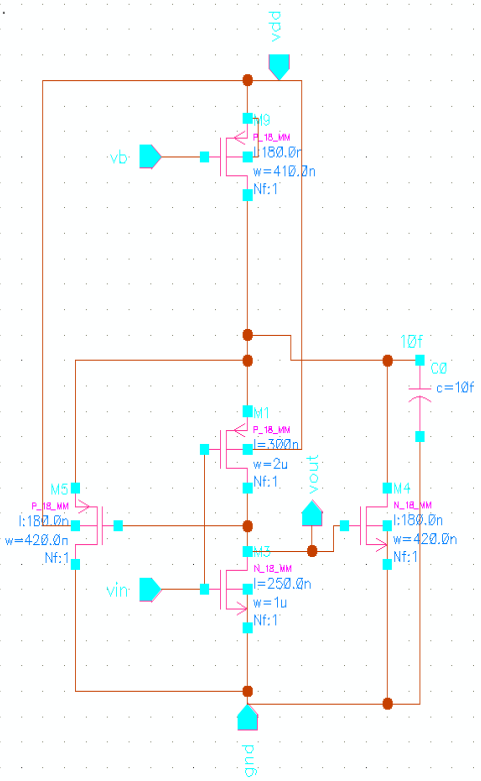

Figure 1: Schematic of CS-CMOS Inverter

CS-CMOS RING OSCILLATOR

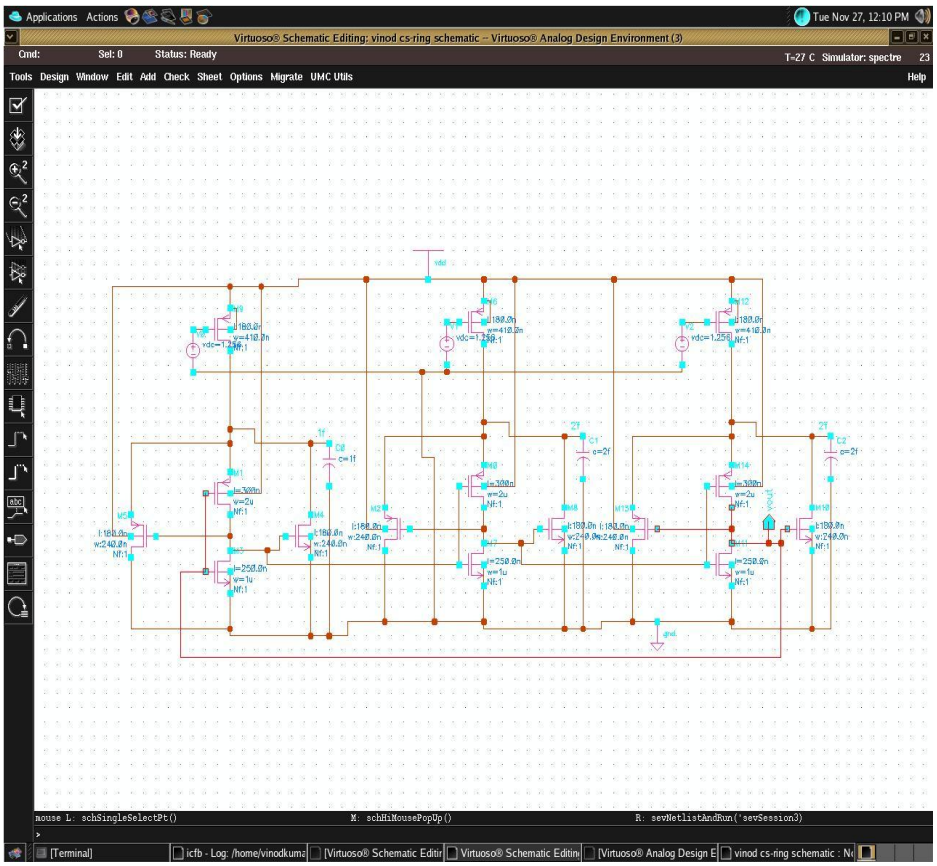

Figure 2: Schematic of CS-CMOS Ring Oscillator

SIMULATION RESULTS

The design of the low noise family ring oscillator is done using Cadence Tool. The Simulation results are done using Cadence Spectre Environment using UMC 0.18. The Table II shows that the simulated results of the low noise family ring oscillator. The p noise response which shows phase noise at offset frequency 1MHz has shown in figure 3, 4, 5 and Figure 6.

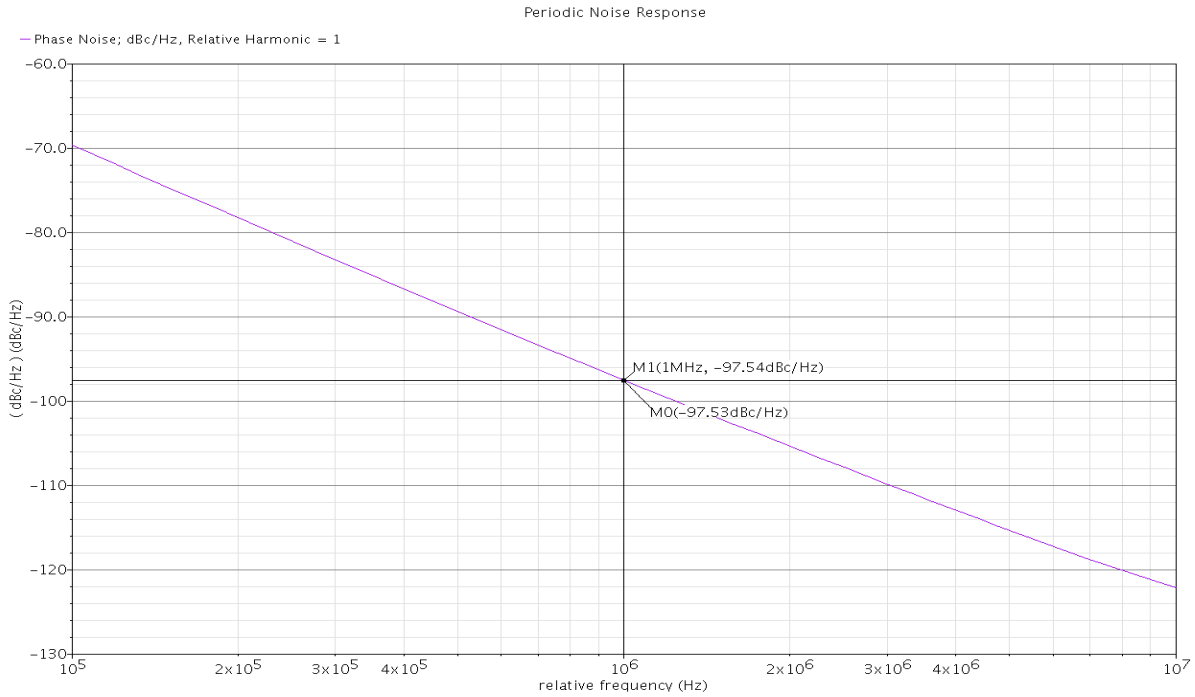

Figure 3: Phase Noise of CS-CMOS Ring Oscillator

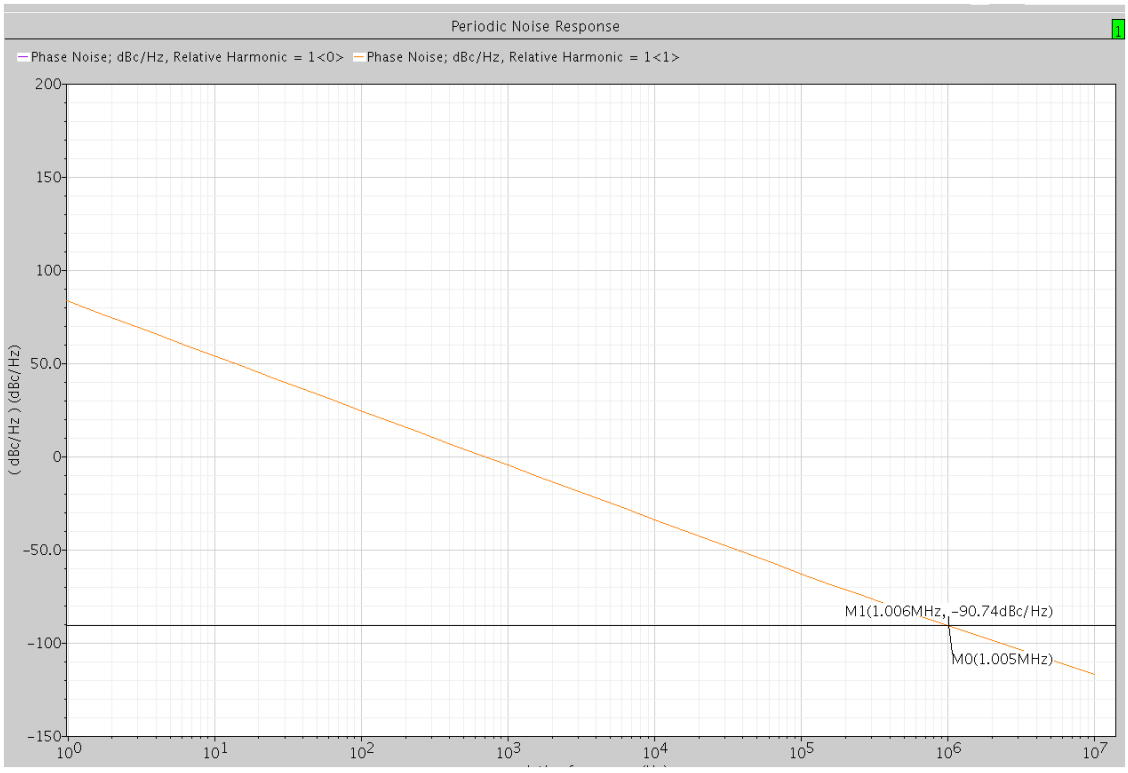

Figure 4: Phase Noise of CSL Ring Oscillator

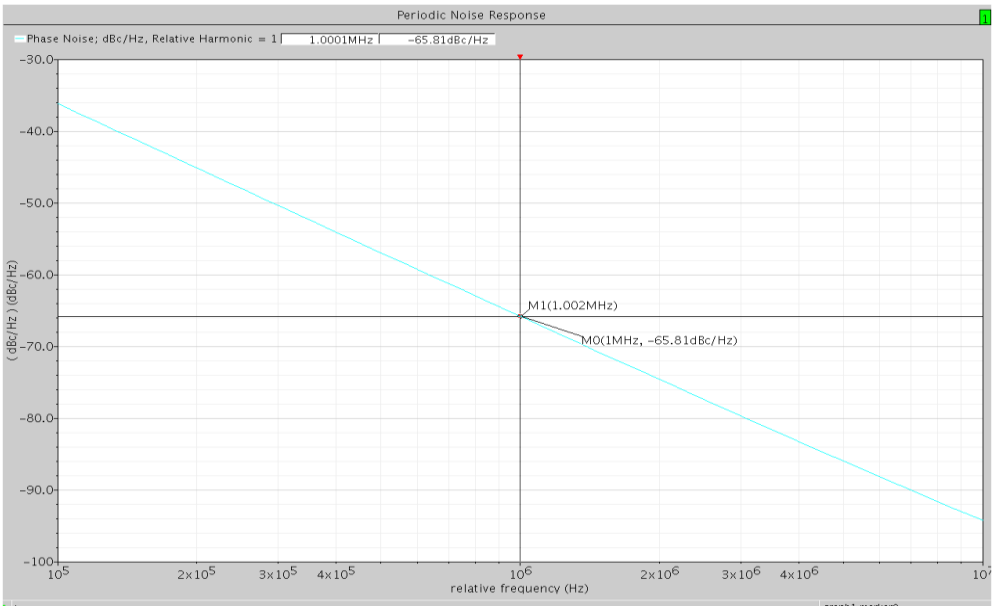

Figure 5 Phase Noise of CBL Logic Ring Oscillator

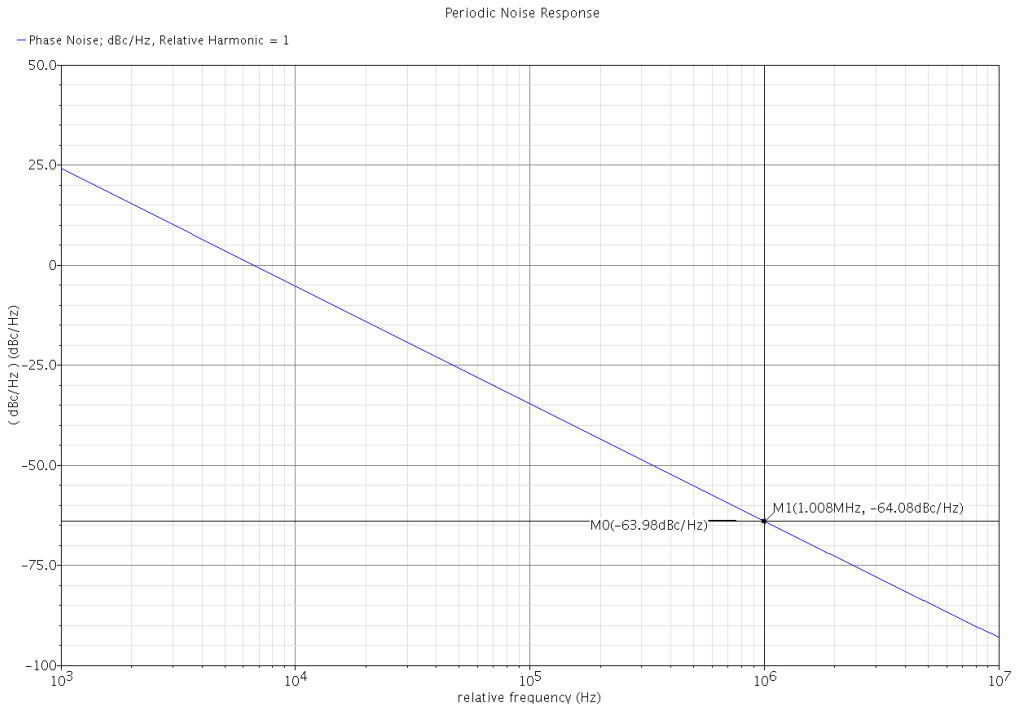

Figure 6: Phase Noise of CMOS Ring Oscillator

Table 1: Phase Noise at 1 MHZ Offset Frequency and Delay

	Simulated Results	
Logic	**Phase Noise**	**Delay Time**
CS-CMOS	-97.54 dBc/Hz	4.2ns
CSL	-90.47 dBc/Hz	8.8ns
CBL	-65.81 dBc/Hz	27.3ns
CMOS	-64.08 dBc/Hz	.18ns

CONCLUSIONS

Design of a low-noise logic CS-CMOS ring oscillator for noise reduction is reported. When it is used in mixed signal integrated systems containing both DSP as well as sensitive analog circuits such as phase-lock loops and data

converters in a single chip of silicon. The new family is obtained by a simple current-steering modification to the standard CMOS logic preserving most of the attractive features of CMOS. The well-known constant-current operation enables a substantial reduction of switching noise. Extensive simulations and measurements demonstrate the speed and power advantages of this family over previously proposed logic families namely CSL and CBL. Each gate uses three additional transistors and a capacitor. However, the circuit configuration improves switching speed around the logical

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