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TWO PHASE INTERLEAVED DC- DC CONVERTER

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ABSTRACT

This paper presents a high-efficiency nonisolated interleaved dc–dc inductor boost converter with a common active clamp circuit. Interleaved boost converters are highly preferred as it reduces the ripple current. A boost converter is used to clamp the voltage stresses of all the switches in the interleaved converter which is caused by the leakage inductances. The leakage energies of the interleaved converters are collected in a clamp capacitor and recycled to the separate load by the clamp boost converter. The proposed converter achieves high efficiency because of the recycling of the leakage energies, reduction of the switch voltage stress, mitigation of the output diode's reverse recovery problem, and interleaving of the converters. Single input given and multiple outputs are taken. Detailed analysis and design of the proposed converter are carried out.

KEYWORDS*:* Conversion Efficiency, Interleaved Dc – Dc Inductor Boost Converter, Onstate Resistance (RDS-*ON),* Power Factor Correction (PFC), Pulse Width Modulation (PWM).

INTRODUCTION

In many industrial applications, it is required to convert a fixed-voltage dc source into a variable – voltage dc source. A dc converter can be considered as dc equivalent to an ac transformer with a continuously variable turn's ratio. Like a transformer, it can be used to step down or step up a dc voltage source. DC converters are widely used for traction motor control in electric automobiles, trolley cars, marine hosts, forklift trucks, and mine haulers. They provide smooth acceleration control, high efficiency, and fast dynamic response. DC converters can be used in regenerative braking of dc motors to return energy back into the supply, and this feature results in energy savings for transportation systems with frequent stops. DC converters are used in dc voltage regulators; and also are used, in conjunction with an inductor, to generate a dc current source, especially for the current source inverters.

The boost converter is widely used in single phase power factor correction (PFC) converters because its input current is continuous and the topology is simple. Most renewable power sources, such as photovoltaic power systems and fuel cells, have quite low voltage output and require series connection or a voltage ooster to provide enough output voltage. High stepup gain, high efficiency and non- isolation are the main characteristics for these applications. Large input current and high- output voltage are the two major concerns for high stepup converters. The high-step-up dc–dc converters can be Non isolated but they should operate at high efficiency while taking high currents from low-voltage dc sources at their inputs. In a conventional boost converter, the duty ratio increases as the output to input voltage ratio increases. However, the previously mentioned applications require highvoltage step-up (step-up ratio 6

or more) and high-efficiency power conversion. Therefore, the conventional boost converters will require extreme duty ratios to meet the highvoltage step-up requirements [3]–[5]. Under such conditions, it is a major challenge to operate the boost converters at high efficiency [6]. This is because, with the high-output voltage, the boost switch has to block a large voltage and hence the ON-state resistance, *RDS*-ON, which varies almost proportionally with the square of blocking voltage, will be very high. Furthermore, the low-level input voltages cause large input currents to flow through the switches. The extreme duty-cycle operation drives short-pulsed currents with high amplitude to flow through the output diodes and the capacitors; which cause severe diode reverse recovery problem and increases in the conduction losses. The high *RDS*-ON of the switches, the increased conduction losses, and the severe reverse-recovery problem will degrade the efficiency and limit the power level of the conventional boost converters [6].

Moreover, the parasitic ringing, present in the practical circuits, induces additional voltage stresses and necessitates the use of switches with higher blocking voltage ratings, which will lead to more losses. The coupled-inductor boost converter [see Fig. 1] can be a good solution to the previously discussed problems of the conventional boost converter. This is because the turns ratio of the primary inductor ($L1$) to the secondary inductor ($L2$) of the coupled inductor can be effectively used to reduce the duty ratio and the voltage stress of the switch. Therefore, for high-voltage step-up applications, the coupled inductor boost converter can be more efficient than the conventional boost converter. However, for high power applications, handling of very large input currents from the low-input voltage sources remains a practical issue. Various converter topologies using magnetically coupled inductors are reported in the literature to reduce to the extreme duty ratio operation for nonisolated high step-up applications [7]–[10]. But they are not suitable for high current and high power applications, and moreover, the circuits are complex to design and model. For high-input current, it can be proposed to interleave the coupled-inductor boost converters to process high power, and to achieve high efficiency and high reliability with reduced size inductors and capacitors [13]. Various advantages of interleaving are well reported in the literature [4], [11], and [12]. An interleaved boost converter with three winding-based coupled inductors is reported in [1], [14] and [15]. This converter has two interleaved phases, and the inductors of one interleaved phase are coupled with the inductors of the other interleaved phase. Therefore, with this converter the modular structure, which is a key beneficial feature of the interleaved converters, cannot be realized. Furthermore, the maximum number of interleaved phases is only two in interleaved converter, presented in this paper, is modular and can be designed for any number of phases. In a practical coupled inductor, there will be considerable amount of leakage inductance present due to the nonideal coupling between the primary inductor ($L1$) and the secondary inductor ($L2$). The leakage inductance (Ll) causes high voltage stresses to the switches, large switching losses, parasitic ringing, and severe electromagnetic interference problems, which degrade the converter performances [6] and [9]. Resistor–capacitor–diode (*RCD*)-based snubber circuits can be used to mitigate the problem, but the losses in these circuits are very high [13] and [10]. Active-clamp circuits can be used to address this issue [10]. But these clamp

circuits are complex and costly. Moreover, the efficiency improvement in these circuits is limited by the high conduction loss in the active-clamp switches [2] and [11].

A diode and capacitor-based passive-clamp circuit is proposed in [1] and [2]. In this clamp circuit, the lamp capacitor (*Cc*) is discharged to the output through the secondary side inductor (*L*2) of the coupled-inductor boost converter [see Fig. 1]. However, the clamp diode (*Dc*), in this circuit, is in series with the coupled inductor. Therefore, it's not only the leakage inductance current, but the total coupled-inductor current, which flows through the clamp diode (*Dc*). This causes large losses in the clamp diode. The clamp diode needs to be rated for the entire large power processed by the coupled-inductor boost converter. This can make the converter operation inefficient for the higher power applications. Furthermore, in this clamp circuit, to take the advantages of the reduced switch voltage stress feature of the coupled-inductor boost converter, the clamp capacitor has to be considerably large, capable of handling the high amount of charge, and discharge currents of the converter. Also, this will cause additional losses in the clamp capacitor. It can be noted that, if any of the previously discussed clamp circuit is used in the interleaved coupledinductor boost converter; each of the interleaved phases of the converter will require additional clamp circuit components and control circuits (for active clamp). This will increase the cost, size, and complexity. A single active-clamp circuit can be proposed, in which the energy stored in leakage inductances of all the interleaved coupled-inductor boost converters are gathered in a common clamp capacitor [1] and [13]. In each of the interleaved units, a clamp diode is connected from the common node of the coupled inductors to the clamp capacitor for providing the discharge path of the leakage energy. Therefore, only the leakage currents flow through the clamp diodes; this makes the clamping operation efficient. A simple boost converter is used to recycle the leakage energy, gathered in the clamp capacitor, to the output of the interleaved converter. The boost converter is controlled to keep the clampcapacitor voltage to a low level, and hence, the voltage stress on the switches is low. This allows the use of low-voltage and high-performance devices. It can be noted that, a conventional boost converter can be used for the clamp circuit, because the ratio of the output voltage to the clamp voltage is not very high.

COUPLED-INDUCTOR BOOST CONVERTER & INTERLEAVING

Coupled-Inductor Boost Converter

Assume that the ideal coupled-inductor boost converter [see Fig. 1] is operating under continuous conduction mode. The waveform of the primary side inductor current or the input current *iL*1 is shown in Fig. 2.

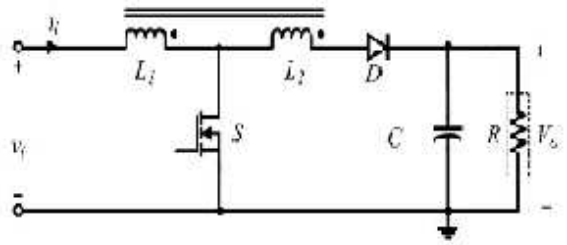

Fig. 1: Coupled Inductor Boost Converter

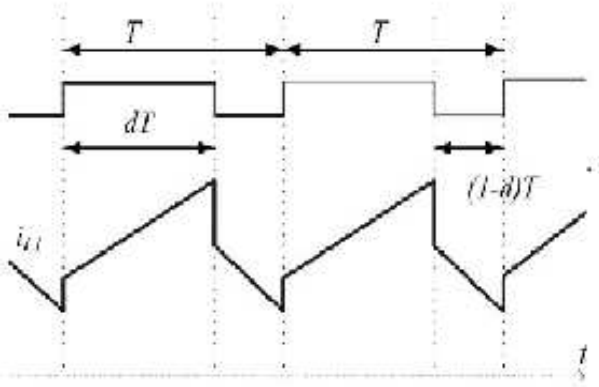

Fig. 2: Gate Pulses and Primary Inductor Current of an Ideal Coupled Inductor Boost Converter

Theoretically, the simplest boost converters and buck converters are able to realise infinite voltage gain with an extreme duty-cycle. However the voltage gain is limited by the parasitic parameters of the power devices, inductor and capacitor. Moreover, the voltage stress of the switch is high, which makes the low voltage high performance devices unsuitable. Furthermore the extreme duty –cycle induces large current ripples, which increase the conduction losses and induce a severe rectifier reverse recovery problem. The high RDS-on switches and the severe reverse –recovery problem degrade the efficiency and limit the power level.

Interleaved Coupled-Inductor Boost Converter

With the increase of the power rating, it is often required to associate converters in parallel. This technique consists of a phase shifting of the control signals of several cells in parallel operating at the same switching frequency. The main advantages are the current distribution, current ripple cancellation, fast transient response and the size of the passive component reduction. So the reliability is increased and high power output is realized.

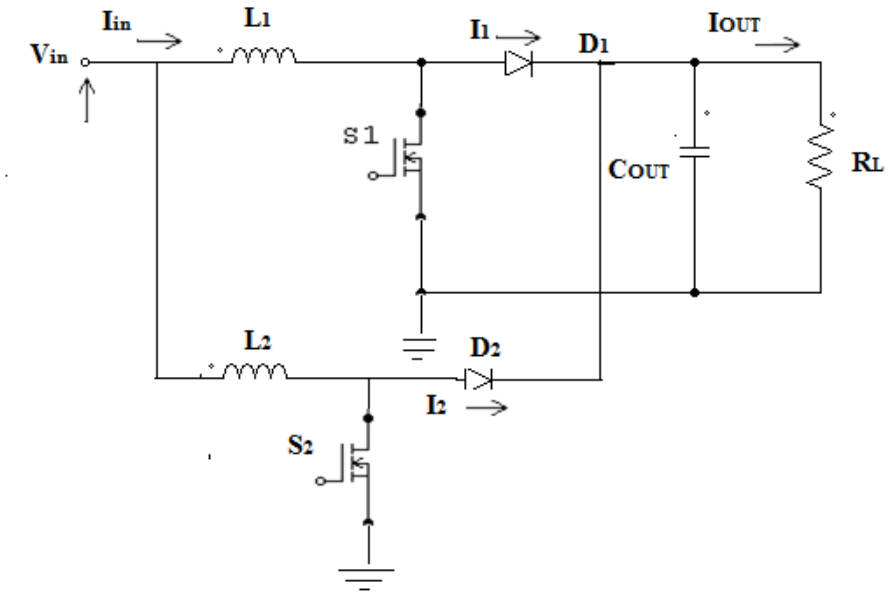

Fig. 3: Two Phase Interleaved Boost Converter

For high current applications, interleaved boost converters are preferable, since the current in the switches are just a fraction of the input current. In addition, interleaved boost converters can also reduce input current ripple and the switching losses, hence the efficiency of the converter is improved. However, the converters are still operated hard switched, resulting in switching losses and the serious electromagnetic interference problems.

Fig. 3 shows the functional diagram of a two phase interleaved boost converter. The interleaved boost converter is simply two boost converters in parallel operating 180° out of phase. The input current is the sum of the two inductor currents IL1 and IL2. Because the inductor's ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current caused by the boost inductors. The best input inductor ripple current cancellation occurs at 50 percent duty cycle. The output capacitor current is the sum of the two diode currents (I1 + I2) less the dc output current. Interleaving reduces the output capacitor ripple current (IOUT) as a function of duty cycle. As the duty cycle approaches 0 percent, 50.

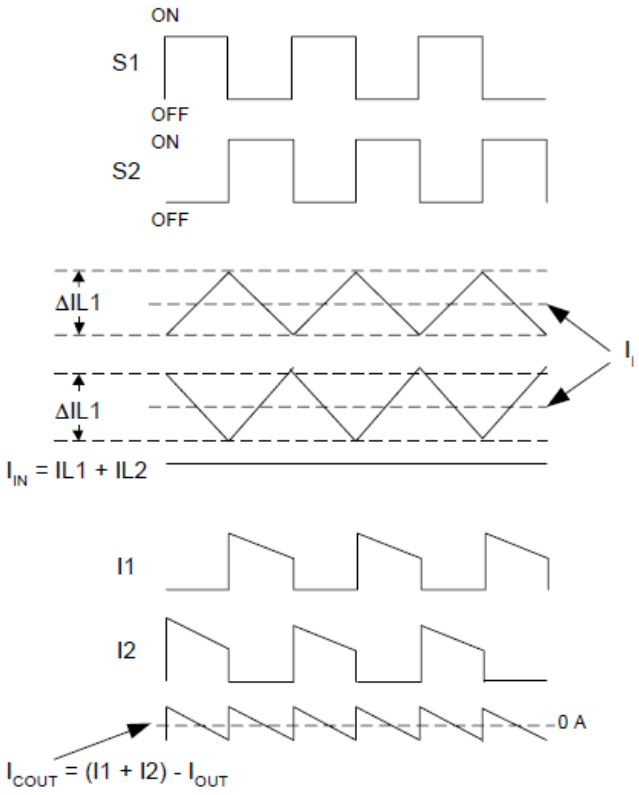

Fig. 4: Waveforms of Interleaved Boost Stage

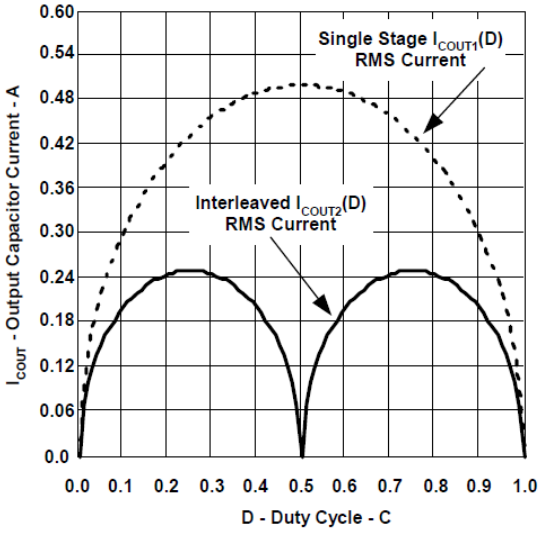

Fig. 5: Output Capacitor RMS Currents as a Function of D Percent and 100 Percent Duty Cycle, The Sum of the Two Diode Currents Approaches Dc. at these Points, the Output Capacitor Has to Filter Only the Inductor Ripple Current. Fig. 4 Shows The Waveforms Of Interleaved Boost Stage.

Interleaving PFC pre-regulator stages has the added benefit of reducing the output capacitor RMS current. Fig 5 shows the normalized output capacitor RMS current in a single stage boost (ICOUT1(D)) and in a two stage interleaved boost converter (ICOUT2(D)) as a function of duty cycle. The RMS current reduces by half. This reduction in RMS current will reduce electrical stress in the output capacitor and improve the converter's reliability.

PROPOSED CIRCUIT & ITS OPERATION

Consider the nonideal coupled-inductor boost converters are operated under continuous conduction mode and a boost converter is used for active clamping of the interleaved converters. Under this condition, there are mainly three modes of operation in one switching cycle of a coupled-inductor boost converter. The operation modes for one of the interleaved phases (Phase-1) are shown in Fig. 6. The nonideal coupled inductors of the interleaved phases can be modeled by a magnetizing inductor (*Lm*1), which is connected in parallel with an ideal transformer and a series leakage inductor (*Ll*1). The turns ratio of the transformer is equal to the primary to the secondary turns ratio (1:*N*) of the coupled inductor. The value of the magnetizing inductance can be obtained by subtracting the leakage inductance value from the primary winding inductance value of the coupled inductor. The input current (*ii*1) and the output current (*io*1) of the interleaved phase are defined in this equivalent model, Fig. 2(a). The key waveforms during the three operation modes are presented in Fig. 2(b). These operation modes are discussed as follow.

Mode-1(*t* □ [*t*0, *t*1]): This mode begins when the switch *S*1 is turned on. The output diode *D*1 is reverse biased, and the input voltage *Vi* charges the primary inductor (*Lm*1) and the leakage inductor (*Ll*1). The rate of rise of the input current of the converter can be written as

$$\frac{di_1}{dt} = \frac{v_i}{L_{m1} + L_{l1}} \qquad t \in [0, dT] \qquad (4)$$

Consider, in steady state, the output power of the Phase-1 of the converter is *Po*1 and the efficiency of the converter is η. The peak input current *Ii*1*P* can be obtained as

$$I_{i1P} = \frac{P_{o1}}{\eta V_i}\frac{1+N}{1+ND} + \frac{V_i}{2}\frac{DT}{L_{l1} + L_{m1}} \qquad (5)$$

Mode-2(*t* □ [*t*1, *t*2]): This mode starts when the switch *S*1 is turned off. The leakage inductor (*Ll*1) forward biases the clamp diode *Dc*1 , and the energy stored in the leakage inductor is discharged to the clamp capacitor *Cc* . This causes a discharge current spike (*icl*1). The peak of this current is equal to the maximum value of the input current (*Ii*1*P*), reached at the end of Mode-1. At the same instant, when the switch *S*1 is turned off, the stored energy in the magnetizing inductor (*Lm*1) forward biases diode *D*1 at the secondary side of the coupled inductor. The voltage difference between the converter output and the input (*Vo* − *Vi*) is divided as per the turns ratio of the ideal transformer and the voltage at the point A [see Fig. 6] is defined below,

$$V_{cl} = \frac{NV_i + V_o}{N+1}$$

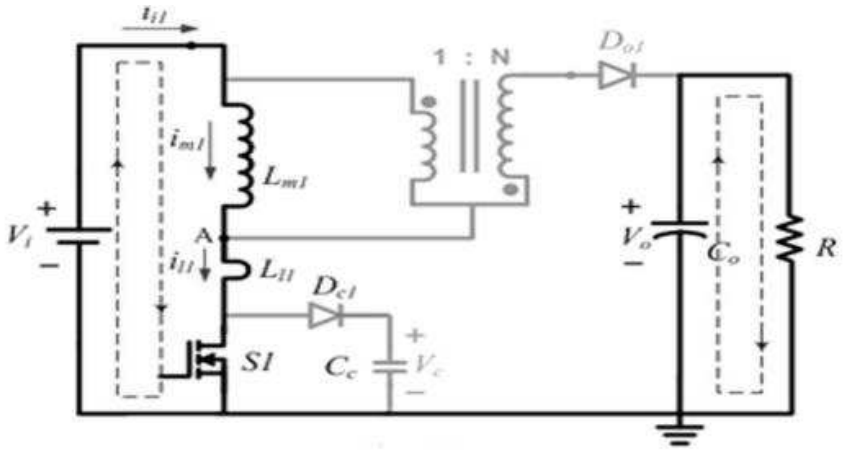

Fig. 6: Equivalent Circuit for Mode 1

It can be noted that the fall rate of the leakage current is decided by the voltage difference between the clamp capacitor voltage *vc* and the voltage the node A. This can be presented by

$$\frac{di_{l1}}{dt} = \left(\frac{Nv_i + v_o}{N+1} - v_c\right)\frac{1}{L_{l1}} \qquad t \in [t_1, t_2] \qquad (6)$$

In steady state, the total fall time for the leakage inductor current *τlf* can be obtained from (5) and (6). This can be defined as

$$\tau_{lf} = \frac{I_{i1P}(N+1)}{V_c(N+1) - (NV_i + V_o)} L_{l1} \qquad t \in [t_1, t_2] \qquad (7)$$

From (6) and (7), it can be seen that the fall time of the inductor current can be reduced by increasing the clamp voltage (*Vc*). These considerations should be taken into account for designing the clamp boost converter and the voltage rating of the switches in the interleaved coupled inductor boost converters. During this mode, the current fall rate in the magnetizing inductor can be found as

$$\frac{di_{m1}}{dt} = \frac{v_i - v_o}{N+1}\frac{1}{L_{m1}} \qquad t \in [t_1, t_2] \qquad (8)$$

The output current (*io*1) and the input current (*ii*1) of the converter can be obtained as

$$i_{o1} = \frac{i_{m1} - i_{l1}}{N+1} \qquad t \in [t_1, t_2]$$

$$i_{i1} = i_{l1} + i_{o1} = \frac{i_{m1} + Ni_{l1}}{N+1} \qquad t \in [t_1, t_2] \qquad (9)$$

Form (9), it can be seen that the slope of the input and the output current of the converter duringMode-2 are defined by the slopes of the magnetizing current (*im*1) and the leakage inductor current (*il*1). As the leakage inductance value is much smaller than the magnetizing inductance value form (6) and (8), it can be seen that the slopes of the input and the output currents in Mode- 2 are mainly decided by the slope of the leakage inductance current.

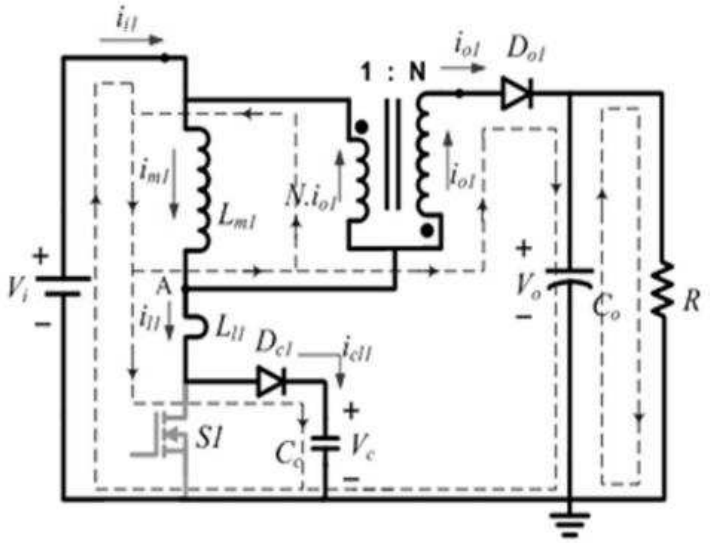

Fig 7 Equivalent Circuit for Mode 2

Mode-3(t □ [t2, t3]): This mode begins when the leakage inductor current (*ii*1) value has become zero, and the leakage energy is completely discharged. The clamp diode *Dc*1 is reversed biased by the clamp voltage *Vc* . The output diode *D*1 remains forward biased and the voltage at the point A is defined by (3). The energy to the output is transferred form the magnetizing inductor and from the source. The switch *S*1 remains turned off.

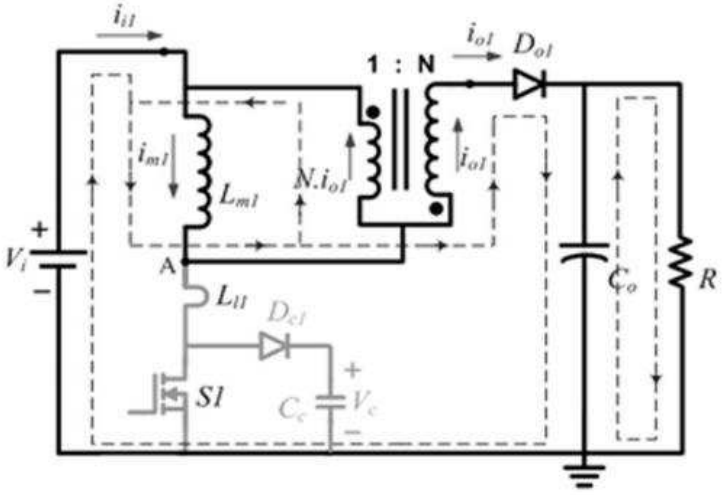

Fig 8 Equivalent Circuit for Mode 3

The Figure 9 shows the Drain-to-source voltage of the switch in a coupled-inductor boost converter without any clamping and Figure 10 shows the output voltage, clamp voltage and drain to source voltage of the switch in a coupled inductor boost converter with the proposed active-clamp circuit.

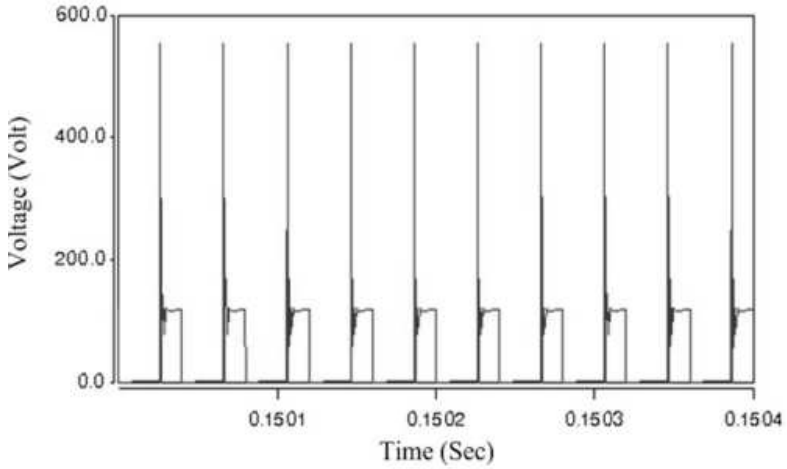

Fig. 9: Drain-To-Source Voltage of the Switch in a Coupled Inductor Boost Converter without Any Clamping

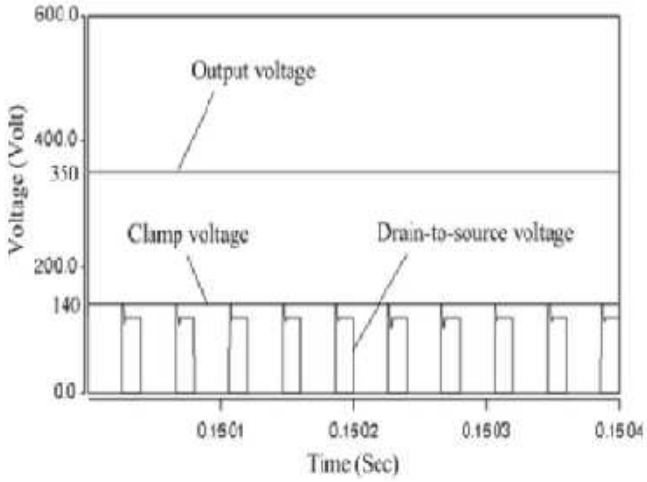

Fig. 10: Output Voltage, Clamp Voltage and Drain to Source Voltage of the Switch in a Coupled-Inductor Boost Converter with the Proposed Active-Clamp Circuit

The circuit is simulated for two phase winding, where the phase shift is 180, using PSIM software and the results are obtained as follows. A 12 to 70V step-up converter with nominal output power rating of 250W is designed and simulated to verify the proposed concept. The converter consists of two interleaved coupled-inductor boost converters and a common clamp boost converter. The estimated leakage inductance of the converter is 1.7 μH. The interleaved converter is designed to operate at a

switching frequency of 25 kHz. The calculated lower limit of the clamp voltage of the designed converter is about 20 V. To limit the fall time of the leakage inductor current to about 2 μs, the clamp voltage level of the converter is designed to be 40 V (5, 7). This clamp voltage value decides the maximum voltage stress of the switches of the coupled-inductor boost converter. The selected MOSFET for the interleaved coupled-inductor boost converter is IR2110 (500 V, *Rds*−ON = 33 mΩ;).In each interleaved phase, four MOSFETs are connected in parallel to realize the switch. The output diode selected for the converter is BY399 (600 V). The simulation results show that the proposed converter can successfully handle the high-input current and perform voltage-step-up operation at a high efficiency. It can be mentioned that if the proposed boost converter based active clamping circuit is not used, the leakage energy cannot be recycled. The energy stored in the leakage inductance is discharged to the clamp-capacitor in the form of a current spike. To clamp the voltage stresses on the switches of the interleaved coupled-inductor boost converters to a low level, the voltage of the clamp capacitor should be maintained at a desired reference value. To achieve this, the clamp-capacitor voltage (the input of the clamp boost converter) is sensed and the clamp boost converter is controlled in a closed loop.

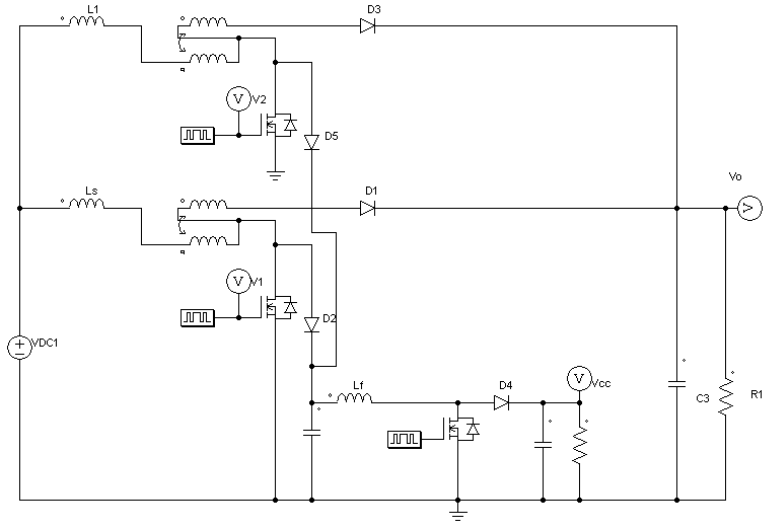

Fig.11: Simulation of Two Phase Winding

The gate pulses for four phase winding is shown in figure 10. They are phase shifted to 90 degree due to interleaving principle. The output voltage, clamp capacitor voltage and the leakage inductance current is shown in the figure 11.

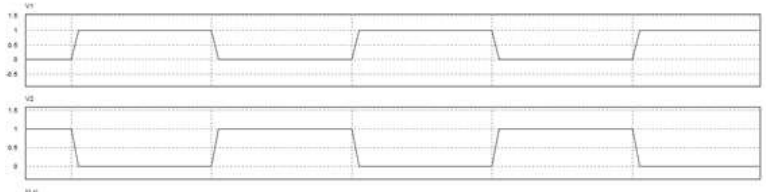

Fig. 12: Gate Pulses for Two Phase Winding

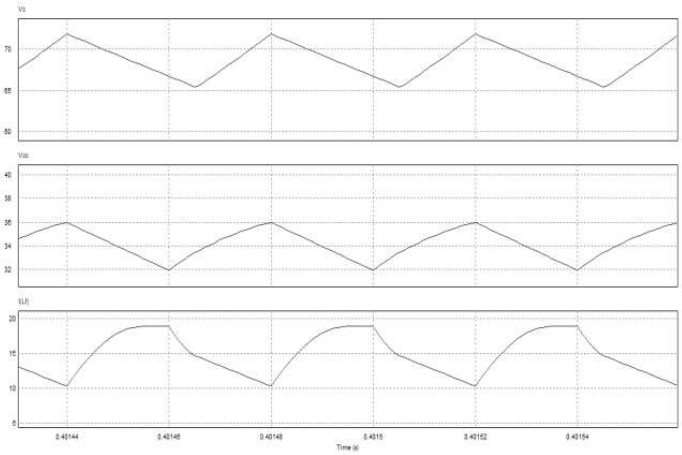

Fig. 13: Waveforms for Two Phase Winding

PROPOSED CIRCUIT HARDWARE OPERATION

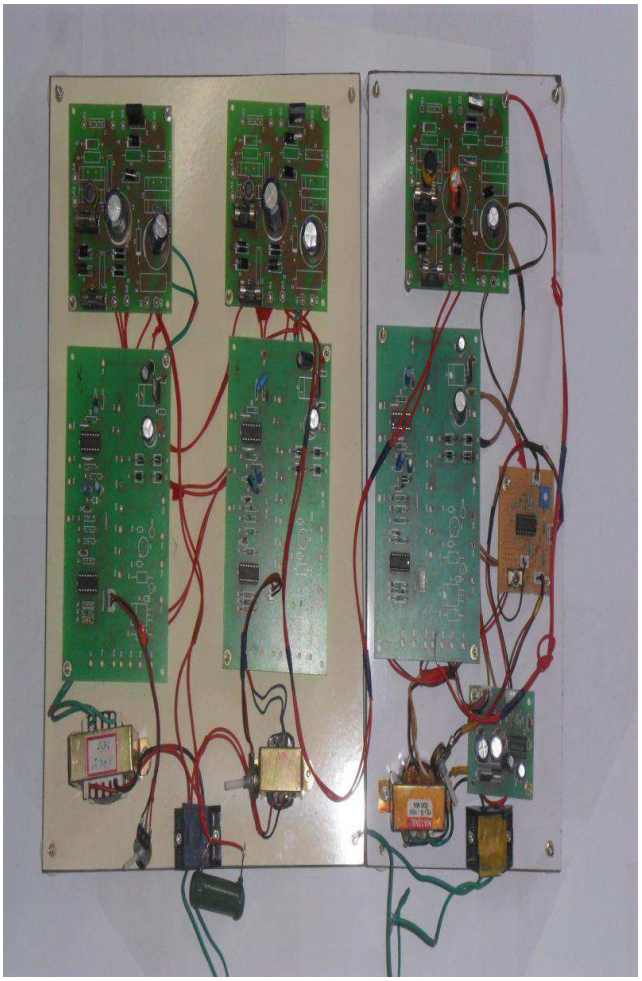

Fig.14: Hardware Design of the Circuit

For the proposed circuit the hardware is done with two phase coupled inductor boost converter. The Controller circuit for the auxiliary circuit consists of triangular wave generator, comparator [op-amp CA3104E] and gate driver IC[IR2110 MOSFETs]. The triangle wave generator generates a triangle wave which is fed to the comparator. The other input to the comparator is a variable rheostat whose value is decided depending on the ripples of the output voltage. The comparator output is fed to gate driver IC which controls the turn on and off of the MOSFETs in the auxiliary circuit. The MOSFETs are turned on and off so as to store the ripple energy from the leakage reactance and then later dissipates the excessive energy to the dc bus. The IR2110/IR2113 is high voltage, high-speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable rugged zed monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output driver's feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an Nchannel power MOSFET or IGBT in the high side configuration, which operates up to 500 or 600 volts. The power circuit consists of PWM rectifier with active ripple storage circuit and a gate drive for the two MOSFETs of PWM rectifier and a separate gate drive for the one MOSFET present in the clamped circuit. A square wave generator is used to generate a square wave. This is fed to the integrator as input to generate the required triangular wave. The rectifier output voltage is controlled by the turn on and off of the MOSFETs by using the gate drive circuit.

Gate drive circuit consists of gate driver ICs [IR2110 MOSFETs] , Triangular wave generator and a comparator IC.[op – amp CA3140E]. Initially square wave generator converts the input dc in to square wave. The square wave is further fed through an integrator circuit which converts the square wave in to triangle wave. The triangle wave is fed to a comparator along with the triangular carrier. The other input to the comparator is the reference input signal. The comparator compares the reference with the triangular carrier and the output of the comparator is fed to a driver IC. The gate driver IC controls the turn on and off of the MOSFETs. The gate pulses for two phase winding is shown in Fig.15. They are phase shifted to 180 degree due to interleaving principle.

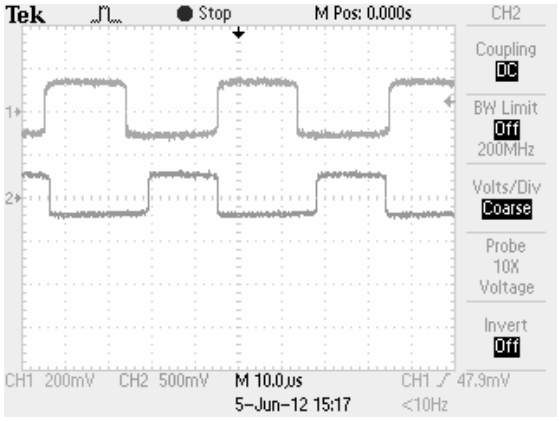

Fig. 15: Gate Pulses for Two Phase Winding

The output voltage for two phase winding is shown in Fig.16. They produce a output voltage of 48.4 V.

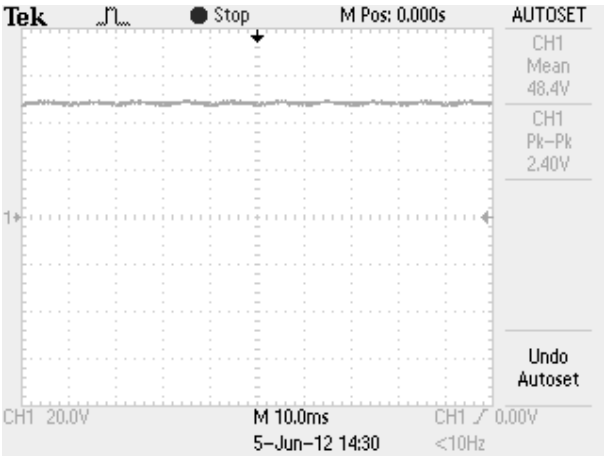

Fig.16 Output Voltage Waveform for Two Phase Winding

The Fig.17 shows the comparison of gate pulse for two phase winding between the simulation output and the hardware output. The simulation output has a exact phase shift of 1800 but the hardware output is not having exact phase shift due to analogue controller.

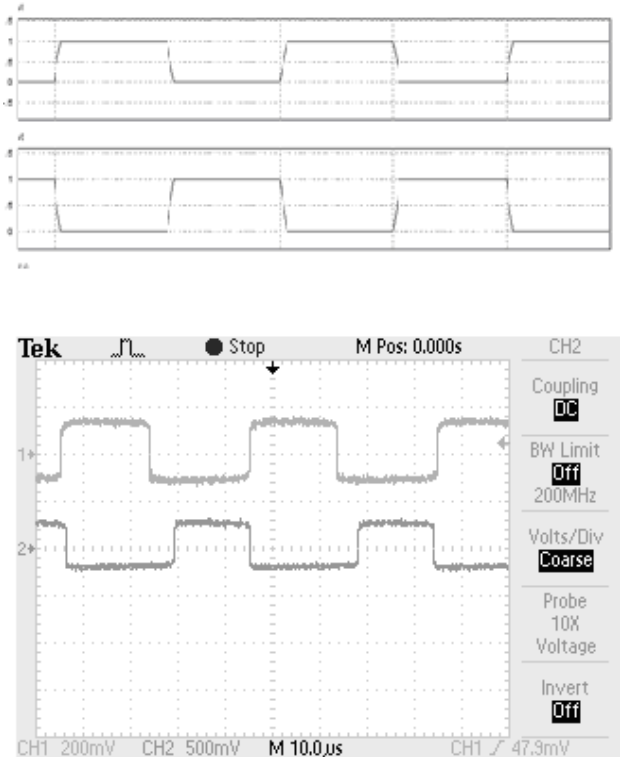

Fig.17 Comparison of Gate Pulses for Two Phase Winding

The Fig.18 shows the comparison of output voltages for two phase winding between the simulation output and the hardware output. The simulation output is showing output voltage as 70 V but the hardware output is having only 50 V as the output. This deviation of 20 V is due to difference in the phase shift of gate pulses. This difference is due to the use of analogue converter. This can be reduced by using microcontroller instead of PID controller

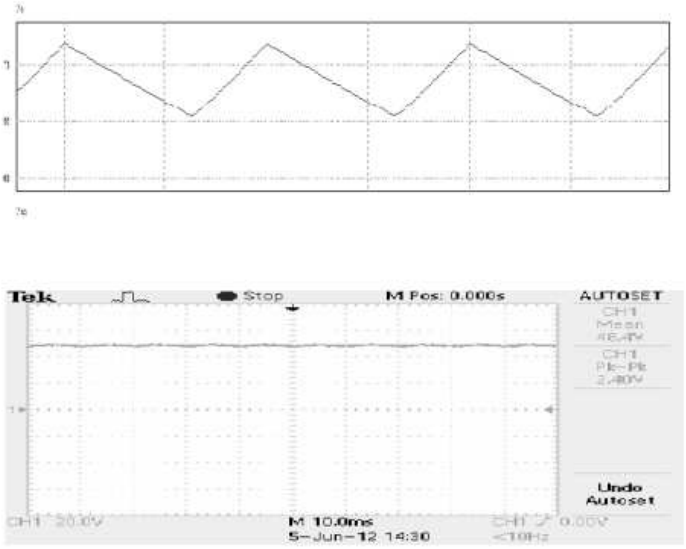

Fig. 18: Comparison of Output Voltages for Two Phase Winding

CONCLUSIONS

The project has proposed a topology based on interleaved coupled inductor boost converter that achieves high efficiency. The leakage energies of the interleaved converters are collected in a clamp capacitor and are collected separately. A boost converter is used to clamp the voltage stresses of all the switches in the interleaved converter. The simulation results for the steady state operation using PSIM version 9.0 have been presented in this report. Hardware verification and theoretical analysis is carried out and the deviation present in the output can be cleared by using microcontroller.

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