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DESIGN AND IMPLEMENTATION OF SAMPLING RATE CONVERSION SYSTEM FOR ELECTROENCEPHALOGRAM (EEG) ON FPGA DEVICE

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ABSTRACT

The wide scale use of digital communication and digital media have made the necessity of methods to process digital data more important now-a-days. The signal-rate system with digital signal processing has evolved the key of fastest speed of digital signal processor. Field Programmable Gate Array **(***FPGA***)** *offers the best solution for addressing the needs of high performance DSP systems. The focus of this paper is on Sampling Rate Conversion (SRC) and DSP functions, namely filtering signals to remove unwanted frequency. This concept leads to a chip with attractive features like, low requirements for the coefficient word lengths, significant saving in computation and storage requirements results in a significant reduction in its dynamic power consumption. This paper introduces an efficient FPGA realization of multi rate decimation filter with a narrow pass - band and a narrow transition band to reduce the frequency sample rate by factor L/M which is applied to generate the bio-signal like EEG signals.*

KEYWORDS: *Bio-Chip, Multi-Rate, Decimate, Interpolate, EEG*

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1. INTRODUCTION

Electroencephalogram (EEG) is a signal with electrical activities for the study of human cognition states. The measurement of these electrical activities can be taken from standardized channel; locations on the scalps [1]. The EEG signal contains noises and artifacts during the recording of the EEG signal. The noise from the main source like *electrooculogram*(EOG), electrocardiogram (ECG), electromyogram (EMG) and other sources should be eliminated to increase accuracy of bio signal processing in bio-chip system. However, there is no need to consider high speed processing and has no effect on the analysis data with a minimum delay of the data measurement procedure [2], [3]. For real time EEG signal analysis, it is argued that software processing is not sufficient and hardware processing needs to be involved. Hardware processing is fast and can provide portability due to its small size. However, it may produce less accurate results than the software processing because of the appearance of quantization errors [4] [5].

The most of the bio - system has got physiological artifacts due to the variety of body activities such as body movements, skin resistance fluctuations or other bioelectrical potentials. From this aspect researcher raise the question how to develop digital filter chip to remove these artifacts. The FPGA is employed in the analysis of EEGs in this project to

perform smooth EEG signal based on the proposed sampling rate conversion system. The proposed multirate system works with sampling rate conversion for high speed data and lower time resolution. The main concept of this design is used to change the sampling rate of a signal. The process of decreasing the sampling rate is called decimation, and the process of increasing the sampling rate is called interpolation [6]-[13].

The main approach of this system is to change the sampling rate of the EEG signals and convert it back into analog and re-digitize it at a new rate. The quantization and aliasing errors inherent in digital-analog-digital conversion processing, would degrade the signal. This paper uses Sample Rate Conversion (SRC) for changing the sampling frequency of a signal digitally. For example, much of the anti-aliasing and anti-imaging filtering in real-time DSP systems can be performed in the digital domain, enabling both sharp magnitude frequency as well as linear phase responses to be achieved.

The system has a computer where the design can be programmed and simulated on Xilinx@ Integrated Software Environment (ISE) Suite 14.7 or Quartus II software with interface ALTRA Cyclone DE II board of FPGA device [14].

This paper is organized as follows. A brief description of materials and methods for the design and implementation of bio chip based on sampling rate conversion obtained experimental results are analyzed and consequent issues are discussed. Finally, conclusions are made.

II. MATERIALS AND METHODS

A. Database

The raw EEG data of signals are collected from the BME signal processing lab from Department of Biomedical Engineering. The data (EEG) are taken on *bypass system* and has been collected from this software for further processing. The patient age was around 28 and all of them were students. The condition for recording EEG signal was solving puzzles. This raw data has included some artifacts into the EEG signals.

B. Proposed Methodology of Multi Rate System

The proposed Multirate system has been considered on sampling rate conversion (SRC) for biomedical signal processing applications. The way to SRC is to connect an ADC in series with a DAC to first convert the continuous signal x(t) to sequence x[n] and then back into the time domain at the new sampling rate $f_{s,new}$. There are three kinds of SRC: decreasing sampling rate (called Decimation where$f_{s,new} < f_{s,old}$), increasing it (called Interpolation where$f_{s,new} > f_{s,old}$),synchronizing two signals with the same sampling frequency ($f_{s,new} = f_{s,old}$). Here, we have considered two different cases as shown in Figure 1 where the sampling rate of signal x[n] is increased by sampling rate L,then filtered using digital filter and after that decreasing the sampling rate by sampling rate M, where for case(i) *L=M*; and case (ii) $L \neq M$.

Case I

A simple block diagram representation of the proposed sampling rate conversion system is given in Figure 1 where h(n) is an anti-aliasing digital filter. This proposed system considers proposed direct form of digital filter implementation, the output of the filter, y(n) and the input x(n), the filter equation is as follows,

$$y(n) = -\frac{3}{35}x(n) + \frac{12}{35}x(n-1) + \frac{17}{35}x(n-2) + \frac{12}{35}x(n- \quad 3) - \frac{3}{35}x(n-4) \qquad \textbf{(1)}$$

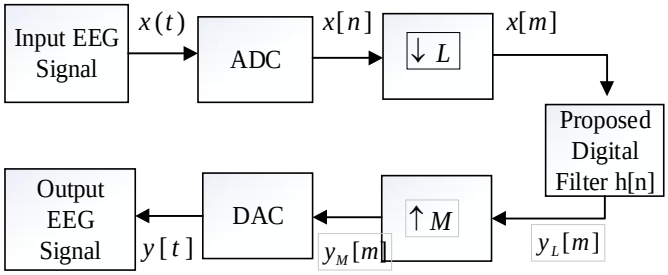

Figure 1: Block Diagram of Proposed Multi Rate System for Case I

The proposed Multirate system has assigned some parameters on input-output relationship for each block as in Figure 1 and its signal flow graph is shown in Figure 2. For every input sample, x(n) fed into the interpolator, after interpolation there are L-1 zero valued sample within sample x(n).These are then filtered using digital filter to yield y(m). Thus, for each input sample for x (n), L samples of y(m). Effectively, the input sampling frequency is increased from f's to Lfs by the interpreter. One implication of inserting L-1 zeroes after each sample is that the energy of each input sample is spread across L output samples. Thus the interpolator has a gain of 1/L. After interpolation , each output samples should be multiplied by L to restore its proper level.

Each input sample fed in, three samples are computed. The non zero samples (that is the actual samples of x (n) in the delay line are separated by L-1 zeroes). Clearly, multiplication operations by the zero valued samples are unnecessary.

We have found the interpolation equation is

$$\mathbf{x}(n) = \mathrm{x}\left(\frac{n}{L}\right) \quad \textbf{(2)}$$

Now the equation (1) can be re written for up sampling as,

$$y_L\left(\frac{m}{L}\right) = y_L(m) = -\frac{3}{35}x\left(\frac{n}{L}\right) + \frac{12}{35}x\left(\frac{n}{L}-1\right)$$

$$+\frac{17}{35}x\left(\frac{n}{L}-2\right)+\frac{12}{35}x\left(\frac{n}{L}-3\right)-\frac{3}{35}x\left(\frac{n}{L}-4\right)$$

Decimation equation is

$$x(n) = x(nM) \quad \textbf{(3)}$$

Now the down sampling equation is,

$$y_M(m) = \mathrm{y_L}(mM) = -\frac{3}{35}x\left(\frac{nM}{L}\right)+\frac{12}{35}x\left(\frac{nM}{L}-1\right)+\frac{17}{35}x\left(\frac{nM}{L}-2\right)+\frac{12}{35}x\left(\frac{nM}{L}-3\right)-\frac{3}{35}x\left(\frac{nM}{L}-4\right)$$

The input $\mathrm{y_L(m)}$ is fed into the delay line one sample at a time. For every M samples of $\mathrm{y_L(m)}$applied to the delay line one output sample$y_M[n]$. This involves keeping the first sample of $\mathrm{y_L(m)}$, discarding the next M-1 samples, keeping the next sample, and discarding the next M-1 samples, and so on. Since for each sample that is kept, the next M-1 samples of $\mathrm{y_L(m)}$ are discarded, it is necessary to perform by the equation (2) for those samples of $\mathrm{y_L(m)}$ that are discarded.

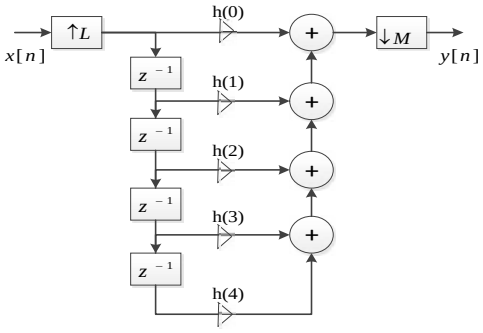

Figure 2: The Signal Flow Graph of Proposed Multi Rate System

Case II

In this case, we have used a system like Figure 1, but in this case, $L \neq M$

C. Flowchart of Multirate System Architecture

Figure 3 shows a flowchart for the proposed sampling rate conversion system operations for case I with interface ALTERA Cyclone DE II Device using processors EP2C35F672C6. For up sampling operations the input EEG signal is converted to binary by ADC and up sampled or interpolator by L which is also in binary. In this implementation, only the non zero valued samples are fetched and used in the computation of the output samples.We see that, at each sampling instant into digital filter, we must first shift the data by one place, read and save the latest input sample, x[n] and compute the current output sample using the difference equation (2). We also used the difference equation (3) for the operation of down sampling by M and use DAC to get output y(t). For the case II we just use reverse operation of L and M into the flow chart.

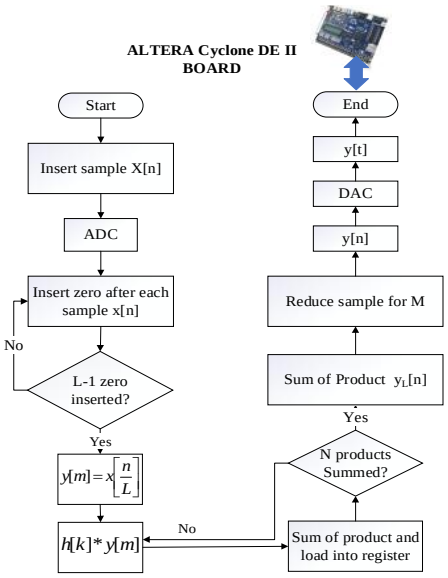

Figure 3: A Simplified Flowchart of Proposed Multi Rate System with Interface ALTERA Cyclone DEII Board

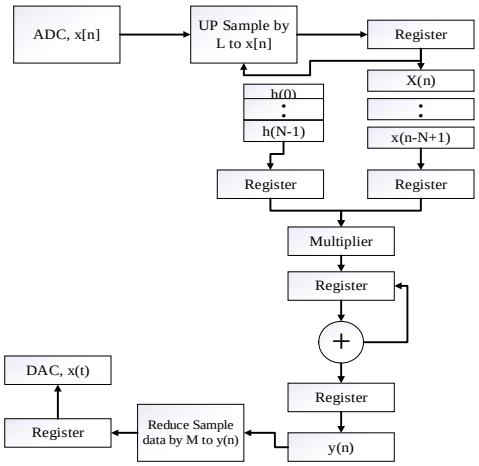

Figure 4: Pipeline MAC Configuration of Proposed Sampling Rate Conversion System

Figure 4 shows pipelined MAC configuration of the proposed system for executing the sampling rate conversion system using equation (2) and (3).

- The arithmetic operation of the proposed multi rate system can be expressed in three distinct steps**:** memory reads, multiply and accumulates**.**
- Adds the previous product to the accumulator**-** initially, the product is zero**.**
- EEG signal decimal data are converted by ADC and stored x**[**n**]** data into auxiliary register**.**
- Increase the discrete samples data of x**[**n**]** by L **(**Interpolator**)** and stored L*****x**[**n**]** data into auxiliary register**.**
- The coefficients a_k by the data memory $x[n]$accessed sequentially and applied to the multiplier**.** The products are summed in the accumulator and store into an auxiliary register **(**AR**).** Initially AR point's $x[$ $]$and ththen, successivelypoints $x[n-$ $]$ decrement the address by 1 where we have used D flip flop for shift register operation for unit delay of samples**.**
- Store sampled filtered output $y_L(n)$ into ra register
- Decrease the sampling rate of $y_L(n)$ M ($y_L(n)/M$) and store within the register**.**
- Finally, we get discrete output$y(n)$ and store it into the register**.**
- Then apply DAC of y[n] and get the values of y**(**t**).**

D. Processing of Algorithm for Proposed Multirate System

For real time digital filtering, the data x[n] and coefficients h[n] are stored in memory, conceptually. At first the data x[n] is increasing the sample by the factor L. If we consider EEG signal elements as illustrate follows are

$$x[n] = [1,2,3,4,5,6,7,8,9,\ldots.]$$

Up-sample by L=2 of x[n], it will happen as

$$x[n] = [1,0,2,0,3,0,4,0,5,0,6,0,7,0,8,0,9,\ldots.]$$

These sequences are applied to digital filter. To appreciate how the digital filter works,consider the simple case of

N=4, with the following differential equation by :

$$y(n) = \frac{-3}{35}x(n) + \frac{12}{35}x(n-1) + \frac{17}{35}x(n-2) + \frac{17}{35}x(n-3) + \frac{-3}{35}x(n-4)$$

where $x(n)$ represents the latest input sample, $x(n-1)$ the last sample, and $x(n-2)$ the sample before last.

Suppose the four-coefficients digital filter is fed from an ADC. The first thing to do is to allocate two sets of contigious memory locations (in RAM), one for storing the input data $(x(n), x(n-1), x(n-2), x(n-3), x(n-4))$ and the other for the filter coefficients $(h(0), h(1), h(2), h(4))$ as depicted below:

Table 1

Data in RAM	Coeeficients in Memory
$\frac{-3}{35}$	$h(0)$
$\frac{12}{35}$	$h(1)$
$\frac{17}{35}$	$h(2)$
$\frac{12}{35}$	h(3)
$\frac{-3}{35}$	h(4)

At initialization, the RAM locations where the data samples are to be stored are set to zero. The following operations are then performed:

- ***First Sampling Instant:*** To read data sample from the ADC and then up-sampled by L into x[n], shift data RAM one place (to make for the new data), to save the new input sample, compute output sample from Equation (7) and then to send the computed output sample and the DAC before down-sample by M.

Table 2

Data in RAM	Coefficients in Memory	
$x(1)$	$\frac{-3}{35}$	$y(1) = \frac{-3}{35}x(1) + \frac{12}{35}x(0) + \frac{17}{35}x(-1) + \frac{12}{35}x(-2) + \frac{-3}{35}x(-3)$
$x(0) = 0$	$\frac{12}{35}$	
$x(-1) = 0$	$\frac{17}{35}$	
$x(-2) = 0$	$\frac{12}{35}$	
$x(-3) = 0$	$\frac{-3}{35}$	

- ***Second Sampling Instant:*** Repeat the above operation and work out sample and send to the DAC.

Table 3

Data in RAM	Coefficients in Memory	
$x(2)$	$\frac{-3}{35}$	$y(2)=\frac{-3}{35}x(2)+\frac{12}{35}x(1)+\frac{17}{35}x(0)+\frac{12}{35}x(-1)+\frac{-3}{35}x(-2)$
$x(1)$	$\frac{12}{35}$	
$x(0)=0$	$\frac{17}{35}$	
$x(-1)=0$	$\frac{12}{35}$	
$x(-2)=0$	$\frac{-3}{35}$	

- ***nth Sampling Instant:*** Repeat the above operation and work out sample and send to the DAC.

Table 4

Data in RAM	Coefficients in Memory	
$x(5)$	$\frac{-3}{35}$	$y(n)=\frac{-3}{35}x(n)+\frac{12}{35}x(n-1)+\frac{17}{35}x(n-2)+\frac{12}{35}x(n-3)+\frac{-3}{35}x(n-4)$
$x(4)$	$\frac{12}{35}$	
$x(3)$	$\frac{17}{35}$	
$x(2)$	$\frac{12}{35}$	
$x(1)$	$\frac{-3}{35}$	

III. EXPERIMENTAL RESULTS ANALYSIS

The methodology described in above sections which are implemented by The ALTRA DE2 FPGA device and Quartus II software which supports devices family, Cyclone II FPGA Kit and also the Xilinx ISE 4.7 design suite. By implementing the processes, the main working procedures are to find out the flowchart simulation, analyze the RTL block diagram, timing diagram and find out its operating parameters. Finally, the results will show best case.

A. Flowchart and Algorithm

The flowchart has been described in section II (C) for the case I. There are three parts which are up-sampling, digital filter design and down-sampling process. All these processes are described below in sections.

i)Up-Sampling

The Figure 5 illustrates the flowchart of the up-sampling process was used in both cases. We have used the raw EEG data that were described in section II. The simulation program has considered a few parameters to execute the total up-sampling procedures. Data are stored in 8-bit registers.

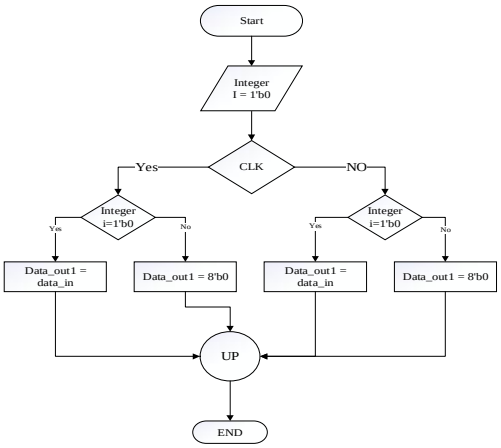

Figure 5: Flowchart of the Up-Sampling Process using Xilinx

The main motto in this operation is to increase the sampling rate of signal. For example, if the sequences of the samples of EEG signal are like (1,2,3,4,5,6……) then the resulting sequences of samples are like (1,0,2,0,3,0,4,0,5,0,6,0…...) for L=2. The advantage of up-sampling is, it can increase the sampling rate of the signal as we wish for detailed processing of the EEG signal. So, by increasing the value of L as we require, we can scrutinize the singnal more precisely for better analysis.

ii) Digital Filter Design in FPGA

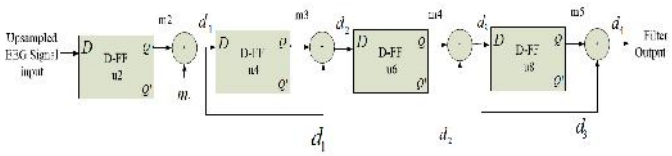

Figure 6: Basic Diagram of Designed Digital Filter Operations

Figure 6 illustrates the basic block diagram of the digital filter. In this block, we have used four D flip flops for 4-unit delay operations. At first, the input is used up-sampled values x [m] which was stored in the registry. These up-sampled values are processed with the following procedures as described below. The EEG data signals which are up sampled are the direct input considered as m_1.

- The 2nd D flip flops input is d_1 = {m_2(output of the 1st D flip flop) + m_1}

  Output = m3

- The 3rd D flip flops input is d_2= {$d_1(m_1 + m_2)$ +m_3(output of the2nd D flip flop)}

  Output = m_4

- The 4th D flip flops input is d_3= {m_4(output of the 3rd D flip flop) +d_2}

  Output = m_5

- The final output = d_4 ={m_5(output of the 4th D flip flop) +d_3}

iii) Down-Sampling

Figure 7 shows the flowchart of the down-sampling process. Like up-sampling, It has considered some parameters for performing down-sampling operation. These data are stored in 8-bit registers.

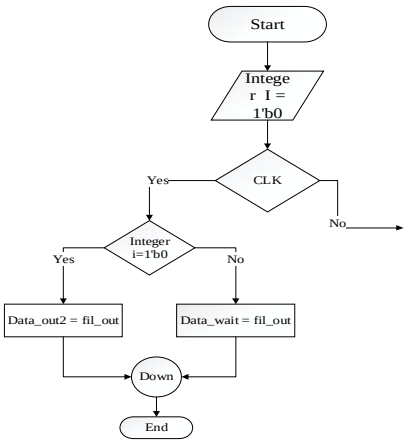

Figure 7: Flowchart of the Down-Sampling Process Using Xilinx

The main aim is to decrease the sampling rate of the filtered signal. For example, if we consider the input sequence of EEG signal like (1,2,3,4,5,6,7,8……) then the down sampled value is like (1,3,5,7…...) for M=2. By increasing the value of M, we can decrease the down-sampling rate for reducing samples as we require. So, down-sampling is the counteraction of up-sampling.

B. RTL Diagram of Sampling Rate Conversion System

In the early stage, registers have been used to perform up-sampling operations. For every clock pulse, an input data has been taken and the input is stored in an intermediate register. Next, data containing zero value is inserted into register within the next clock pulse. The Section-1 (rectangle) of Figure 8 shows the up-sampler connection of RTL block.Furthermore, for digital filter operation, we have used D flip-flops as memory element and it has connected four D Flip-flops in series in order to obtain the Shift Register operation where input clock and reset value controls the D flip-flops. Section-2 (rectangle) of Figure 8 shows the RTL diagram of digital filter. Finally, The Down-sampling operation is performed by again using registers. Section-3 (rectangle) of Figure 8 shows the down-sampling operation section. Within the RTL block, multiplexers (MUX 2:1) andLookup tables(4-LUT) have been used to generatelogic operations. Here, registers have been used to store each and every data. Again,multipliers, 8-bit adders, latches are used in the RTL diagram as shown inTable-5 below. Next, Table 6 shows that the core temperature was 27.2°C during the simulation process. Table 6 also shows the voltage supply (V_{cc}), total current and total power needed for the proposed system design.

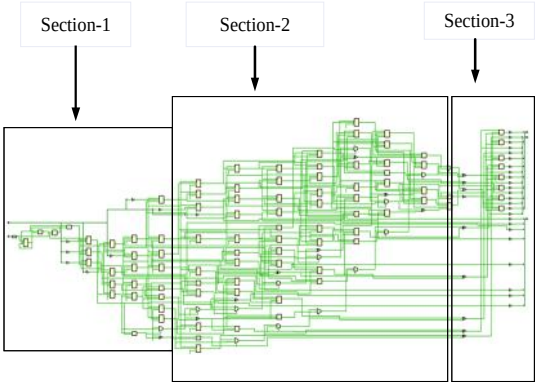

Figure 8: RTL Diagram for Sampling Rate Conversion System

Table 5: HDL Synthesis Report (Macro Statistics)

Multipliers	3
8x2-bit multiplier 8x3-bit multiplier	2 1
Adders/Sub-tractors (8-bit adder)	4
Registers(D Flip-Flops)	72
Latches (8-bit latch)	1
IOs	33
Total No. of Paths	**32**

Table 6: Power Analyzer Report of Sampling Rate Conversion System

Coretemp	27.2°C
Voltage supply(v_{cc})	2.4V
Total Current (A)	0.016A
Total Power(W)	0.08W

C. Timing Diagram

The timing diagrams of Figures 9 and 10 illustrate different cases. The Figure 9 shows the case I where we have used $L = 2$ and $M = 2$. In this case I we have mentioned the result parameters in Figure 9 that we have simulated in proposed design operations. The data input as $x[n = 0]$indicted as well as data upsampled by $L = 2$ between input data $x_{L(1)}(m = 0) = 38$ up-sampled data as$x_{L(2)}(m = 0) = 0$within the single clock pulse. The filtered output data shows with respsect to input data $x_{L(1)}(m = 0) = 38$, the filtered output up-sampled data $y_{L(1)}(m = 0) = 145$ and for up-sampled data $x_{L(2)}(m = 0) = 0$shows $y_{L(2)}(m = 0) = 85$ within the same single clock pulse. The final filter out shown after down-sampling operation by $M = 2$ which shows as $y_m(m = 0) = 84$ after one clock pulse shift. Figure 10 shows timing diagram for case II $(L = 3, M = 2)$.

The Table 7 shows the timing summery of proposed design on multi rate system for the case I.

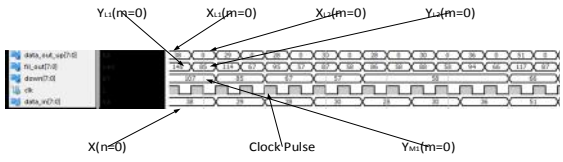

Figure 9: Timing Diagram of L=2 and M=2

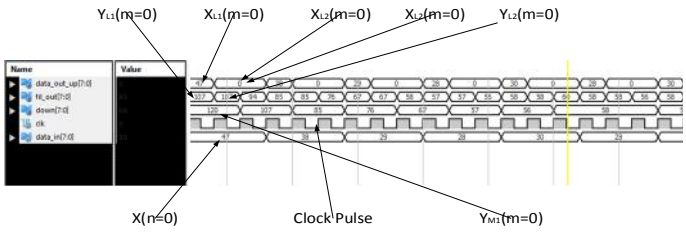

Figure 10: Timing Diagram of L=3 and M=2

D. Result Analysis

Table 8 shows the first 10 EEG data and their corresponding outputs. Here up-sampled data are twice the input data for L=2 & M=2. Again, the up-sampled data is filtered by digital filter & finally we get the down-sampled data which is our desired outputdata. For simulation purposes, we have used 122 EEG data. The comparison of Input EEG data and Output EEG data is shown in Figure 11. It is clear that data have been amplified by the filter.

Table 7: Timing Summary of Sampling Rate Conversion System

Clock period	15.570 ns
Clock Frequency	64.226 MHz
Minimum input arrival time before clock	1.946 ns
Maximum output required time after clock	11.196 ns
Maximum combinational path delay	No path found

Table 8: First 10 Data for L=2 & M=2 Case

SL.	Data Input	Up Sampled Value	Filter Output	Down Sample/Data Out
01	38	38	145	85
		0	85	
02	29	29	114	67
		0	67	
03	28	28	95	57
		0	57	
04	30	30	87	58
		0	58	
05	28	28	88	58
		0	58	
06	30	30	94	66
		0	66	
07	36	36	117	87
		0	87	
08	51	51	140	104
		0	104	
09	53	53	166	115
		0	115	
10	62	62	180	127
		0	127	

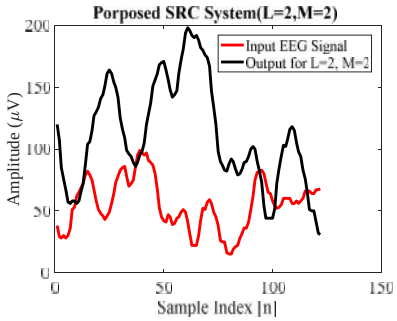

Figure 11: Result Comparison of Input and Output EEG Signals for L=2 & M=2

The Figure 11 illustrates a plot of the EEG data and its final outputs of Sampling Rate Conversion System. In this figure, the raw EEG signal is shown as blue color, green color shows for the case I where L=2, M=2. In figure 12 light magenta color shows input EEG signal and deep magenta color shows the output signal for case II (L=3, M=2). It's clearly observed that sampling rate conversion has worked properly in this proposed system. The results of case I have shown better results than case II. So, it is clear that higher up-sampling and down-sampling rate works better. Case I and II have shown a different way of Multirate operations in proposed system design. The results of case I show better results than case II where case I uses up-sampling first and then down-sampling, case II have shown sample values of EEG data increases than input EEG signal because of using the ratio L/M.

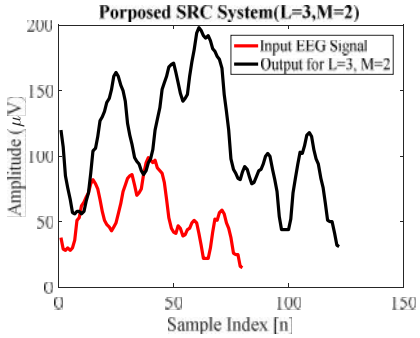

Figure 12: Result Comparison of Input and Output EEG Signals for L=3 & M=2

Figure 13 shows a basic architecture for proposed design on Multirate system using blocks of individual components in case I. The main components are coefficients and data memories, analog input/output units (ADC and DAC), multiplier-accumulator (MAC), and a controller (not shown). The components of this proposed system can be implemented with fast, off-the-shelf products. Similar way we can develop for the case II in terms of change L and M.

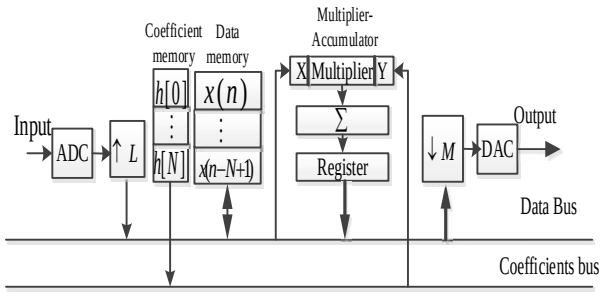

Figure 13: Architecture of Sampling Rate Conversion System for Case I

IV. CONCLUSIONS

We have presented an easy and simple approach, design and implementation sampling rate conversion for EEG signal on FPGA Device. In this system, considered two cases for the justification of the best Multirate based approach of the proposed system. We have also checked the system characteristics such as performance parameters: speed, clock frequency, power consumption on HDL synthesis report, power analysis and timing diagram. In the future, this model can be enhanced and developed with larger datasets to apply into an athlete body monitoring system. So it will be interesting to know how medical technology uses this proposed method in patient monitoring system for simple and fast diagnosis.

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